SPECIFICATION AMENDMENTS

Replace the paragraph beginning at page 2, line 6 with:

Fig. 7B is a cross-sectional view of the strip line portion shown in Fig. 7A taken along line ~~B—B'~~ VIIB-VIIB. As shown in Fig. 7B, the strip line has a 3-metal-layer structure (or a structure including 3 metal layers) in which grounding conductors (hereinafter referred to as GNDs) 105 and 106 ~~are formed such that they~~ sandwich a strip conductor 104 ~~formed~~ within dielectric material.

Replace the paragraph beginning at page 2, line 13 with:

The characteristic impedance of the strip line is expressed by Formula 1.

[Formula 1]

$$(1/4) \times (\mu/\epsilon)^{1/2} \times (b/W),$$

where μ denotes the magnetic permeability and ϵ denotes the dielectric ~~permeability~~ permittivity. Further, the symbol b denotes the distance between the GND 105 and the GND 106, and W denotes the width of the strip conductor 104, that is, the signal line width, as shown in Fig. 7B. It is assumed that the distance of the GND 105 from the strip conductor 104 is equal to that of the GND 106 from the strip conductor 104.

Replace the paragraph beginning at page 3, line 5 with:

On the other hand, the obverse and the reverse surfaces of the substrate of the high-frequency power amplifier may have wiring prohibited areas therein in which wiring for a strip line is prohibited. For example, in a chip component mounting portion of the substrate, the portion of the substrate top surface on which the non-GND terminals of the chip components exist cannot be used as a GND surface. Therefore, the region of the substrate from the chip component mounting portion to the GND surface within the substrate is set as a wiring prohibited area. Fig. 7C is a cross-sectional view of the strip line portion shown in Fig. 7A taken along line ~~C—C'~~ VIIC-VIIC. In the figure, reference numerals 107 and 108 denote wiring prohibited areas.

Replace the paragraph beginning at page 3, line 17 with:

Further, a cavity structure as shown in Fig. 8 also requires a wiring prohibited area. Specifically, since transistors, etc. are mounted on a cavity portion 110 ~~formed~~ in a substrate 109, the cavity portion 110 is ~~set as~~ a wiring prohibited area.

Replace the paragraph beginning at page 7, line 11 with:

Fig. 7B is a cross-sectional view of the strip line portion shown in Fig. 7A taken along line ~~B-B'~~ VIIB-VIIB.

Replace the paragraph beginning at page 7, line 13 with:

Fig. 7C is a cross-sectional view of the strip line portion shown in Fig. 7A taken along line ~~C-C'~~ VIIC-VIIC.